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EXAMINER	
NGUYEN, VAN THU T	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 11/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,469	LEE ET AL.	
	Examiner	Art Unit	
	VanThu Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-5,8,11-12,14-16 is/are rejected.

7)☒ Claim(s) 6,7,9,10 and 13 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 11 March 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 are pending.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

See Abstract, lines 1-2.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 14-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 14, lines 10-13, limitation "transmitting data transmitted to the global read line pair (e.g. RD0) to a local read line pair and outputting data transmitted to the local read line pair through a data output (input) pad during a read operation" is not clear. Do Applicants mean to say -- and transmitting data transmitted to the **local** read line pair (e.g. RD0) to a **global** read line pair and outputting data transmitted to the **global** read line pair through a data output (input) pad during a read operation--?

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-5, 11-12, 14-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Osada et al. (U.S. Patent No. 6,665,209, referring hereafter as Osada) or Hidaka (U.S. Patent No. 6,542,428) or Watanabe et al. (U.S. Patent No. 6,418,067, referring hereafter as Watanabe)

Regarding claim 1, Osada discloses a semiconductor memory device (see FIG. 3) comprising:

a memory cell array (BANK1) including a plurality of memory cells connected between a plurality of word lines (WL) and a plurality of bit line pairs (e.g. LBL0-LBLB0 to LBL3-LBLB3);

a predetermined number of write line pairs (WGBL and WGBLB)

a predetermined number of read line pairs (RGBL and RGBLB)

a plurality of write column selection gates for transmitting data between the plurality of bit line pairs and the predetermined number of write line pairs during a write operation (MN5 and MN6, see FIGS. 1 and 3); and

a plurality of read column selection gates for transmitting data between the plurality of bit line pairs and the predetermined number of read line pairs in response to a read operation (MN3 and MN4, see FIGS. 1 and 3)

Regarding claims 2-3, Osada discloses predecoder and other control circuits are arranged in region 147 (see FIG. 6 and column 8 lines 2-3). It is inherent that control circuit comprising command decoder for decoding externally input command signals and generating a write command for the write operation and a read command for the read operation; and the read and write operations are performed simultaneously [in one clock cycle] (see FIG. 13).

Regarding claims 1, 2 and 4, Hidaka discloses a semiconductor memory device comprising:

a memory cell array (101, see FIG. 2) including a plurality of memory cell array blocks (110, see FIG. 2) each including a plurality of inherently memory cells connected between a plurality of inherent word lines and a plurality of bit line pairs (e.g. BL1-/BL1 to BL4-/BL4, see FIG. 6);

a predetermined number of local write line pairs of each of the plurality of memory cell array blocks for inputting data in each of the plurality of memory cell array blocks (local write line pair LW1 and /LW1 for each block 110, see FIG. 6);

a predetermined number of local read line pairs of each of the plurality of memory cell array blocks for outputting data of each of the plurality of memory cell array blocks (local read line pair LR0 and /LR0 for each block 110, see FIG. 6);

a plurality of write column selection gates of each of the plurality of memory cell array blocks for transmitting data between the plurality of bit line pairs and the predetermined number of local write line pairs during a write operation (write column select gates WCSG1-WCSG4);

read column selection gates of each of the plurality of memory cell array blocks for transmitting data between the plurality of bit line pairs and the predetermined number of local read line pairs during a read operation (read column select gate RGT1-RGT4);

a predetermined number of global write line pairs connected to a predetermined number of local write line pairs of each of the plurality of memory cell array blocks (a global write data bus pair GWDB and /GWDB for memory cell array blocks along one column, see FIGS. 2 and 6)

a predetermined number of global read line pairs connected to a predetermined number of local read line pairs of each of the plurality of memory cell array blocks (a global read data bus pair GRDB and /GRDB for memory cell array blocks along one column, see FIGS. 2 and 6);

Regarding claim 5, Hidaka further disclose a command decoder for decoding externally input command signals and generating a write command for the write operation and a read instruction for the read operation (control circuit 26 receiving external input command signals /RAS, /CAS, /WE and generating inherent read/write command for read/write operations, see FIG. 1).

Regarding claims 11, Watanabe discloses, in FIG. 7, a method for writing and reading data to and from a semiconductor memory device comprising the steps of:

transmitting data input through a first pad (e.g. DB0) to a global write line pairs (e.g. WD0) during a write operation, and data output from a memory cell array to a read line pair during a read operation (e.g. read data from one of the memory block to its corresponding local read data line pairs IOR0-IOR31); and

transmitting data transmitted to the write line pair (e.g. WD0) to the memory cell array during a write operation, and outputting data transmitted to the read line pair through a second pad (e.g. QB0) during a read operation.

(See column 49 line 42 to column 50 line 18)

Regarding claim 12, Watanabe also disclose the read and write operations are performed independently (not simultaneous).

Regarding claims 14, Watanabe discloses, in FIGS. 7-8, a method for writing and reading data to and from a semiconductor memory device comprising the steps of:

transmitting data input through a data input/output pad (e.g. QB0/DB0) to a global write line pair (e.g. WD0) during a write operation, and transmitting data stored in a memory cell array to a local read line pair (e.g. data from one or memory array to its corresponding IOR0-IOR31) during a read operation;

transmitting data transmitted to the global write line pair (e.g. WD0) to a local write line pair (e.g. one of IOW0-IOW31) during a write operation, and transmitting data transmitted to the local read line pair (e.g. one of IOR0-IOR31) to a global read line pair (e.g. RD0) during a read operation; and

transmitting data transmitted to the local write line pair to the memory cell array (e.g. data from one of IOW0-IOW31 to its corresponding memory array) during a write operation, and transmitting data transmitted to the local read line pair (e.g. one of IOR0-IOR31) to a global read line pair (e.g. RD0) and outputting data transmitted to the global read line pair through a data input/output pad (e.g. QB0/DB0) during a read operation.

Regarding claim 15, Watanabe also disclose the read and write operations are performed independently (not simultaneous).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka (U.S. Patent No. 6,542,428) in view of Watanabe et al. (U.S. Patent No. 6,418,067, referring hereafter Watanabe).

Regarding claim 8, Hidaka discloses a semiconductor memory device comprising:

a memory cell array (101, see FIG. 2) including a plurality of memory cell array blocks (110, see FIG. 2) each including a plurality of inherently memory cells connected between a plurality of inherent word lines and a plurality of bit line pairs (e.g. BL1-/BL1 to BL4-/BL4, see FIG. 6);

a predetermined number of local write line pairs of each of the plurality of memory cell array blocks for inputting data in each of the plurality of memory cell array blocks (local write line pair LW1 and /LW1 for each block 110, see FIG. 6);

a predetermined number of local read line pairs of each of the plurality of memory cell array blocks for outputting data of each of the plurality of memory cell array blocks (local read line pair LR0 and /LR0 for each block 110, see FIG. 6);

a plurality of write column selection gates of each of the plurality of memory cell array blocks for transmitting data between the plurality of bit line pairs and the predetermined number of local write line pairs during a write operation (write column select gates WCSG1-WCSG4);

read column selection gates of each of the plurality of memory cell array blocks for transmitting data between the plurality of bit line pairs and the predetermined number of local read line pairs during a read operation (read column select gate RGT1-RGT4);

a predetermined number of global write line pairs connected to a predetermined number of local write line pairs of each of the plurality of memory cell array blocks (a global write data bus pair GWDB and /GWDB for memory cell array blocks along one column, see FIGS. 2 and 6)

a predetermined number of global read line pairs connected to a predetermined number of local read line pairs of each of the plurality of memory cell array blocks (a global read data bus pair GRDB and /GRDB for memory cell array blocks along one column, see FIGS. 2 and 6);

a command decoder for decoding externally input command signals and generating a write command for the write operation and a read instruction for the read operation (control circuit 26 receiving external input command signals /RAS, /CAS, /WE and generating inherent read/write command for read/write operations, see FIG. 1).

However, Hidaka does not discloses the semiconductor memory device comprising write column decoder, read column decoder, data in put circuit, data output circuit.

Watanabe discloses a semiconductor memory device comprising:

a write column decoder for generating write column selection signals to select a predetermined number of write column selection gates among the plurality of write column selection gates by inputting a column address during the write operation (write column decoder WYDa and WYDb for each memory block R#, which generating write column select signals WCSLs via column bank address RBact2, see FIG. 3)

a read column decoder for generating read column selection signals to select a predetermined number of read column selection gates among the plurality of read column selection gates by inputting the column address during the read operation (read column decoder RYDa and RYDb for each memory block R#, which generating read column select signals RCSLs via column bank address RBact2, see FIG. 3)

a data input circuit for transmitting data input to a predetermined number of data input pads to the predetermined number of global write line pairs (data input buffer DB0-DB31 receiving data from data input pad D0-D31 global write line pairs, see FIG. 7);

a data output circuit for outputting data transmitted from the predetermined number of global read line pairs to a predetermined number of data output pads (data output buffer QB0-QB31 receiving data from data input pad Q0-Q31 global read line pairs).

Since Hidaka and Watanabe are both from the same field of endeavor, the purpose disclosed by Watanabe would have been recognized in the pertinent art of Hidaka.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to provide separated read, write column decoders and data input, data

output circuit in a large scale semiconductor for the purpose of perform read and write operation independently from each other and achieve a higher system performance.

Allowable Subject Matter

9. Claims 6-7, 9-10, 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claim 16 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowability:

The prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Hidaka and Watanabe, taken individually or in combination, do not teach the claimed invention having the following limitations, in combination with the remaining claimed limitations:

As in claim 6: wherein the command decoder further decodes the command signals to generate write and read commands for performing the write and read operations simultaneously; or

As in claim 7: a first switch for transmitting data input through a predetermined number of data input pads to the predetermined number of global line pairs in response to a control signal, and outputting data transmitted from the predetermined number of global read line pairs to a predetermined number of data output pads; and a second switch for transmitting data input through the predetermined number of data output pads to the predetermined number of global

line pairs in response to an inverted signal of the control signal, and outputting data transmitted from the predetermined number of global read line pairs to the predetermined number of data input pads.

As in claim 9: wherein the command decoder decodes the command signals and further generates the write and the read commands for performing the write and the read operations simultaneously; or

As in claim 10: a first switch for transmitting data input to a predetermined number of data input pads to the data input circuit in response to a control signal, and transmitting data transmitted from the data output circuit to a predetermined number of data output pads; and a second switch for transmitting data input through the predetermined number of data output pads to the data input circuit in response to an inverted signal of the control signal, and transmitting data output from the data output circuit to the predetermined number of data input pads.

As in claim 13: wherein the write operation and the read operation are performed simultaneously.

As in claim 16: wherein the write operation and the read operation are performed simultaneously.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Friday, 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

November 10, 2005

VanThu Nguyen
Primary Examiner
Art Unit 2824